Electronic Version
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Claims

[c1] A method for selective salicidation of a semiconductor device, the method comprising the steps of:
providing a first structure having an n-type dopant therein and a second structure having a p-type dopant therein;
exposing at least the first structure to an ozonated water bath; and
salicidizing the first and second structure whereby silicide is formed only over the second structure.

[c2] The method of claim 1, wherein the ozonated water bath includes no less than approximately 1 parts per million (ppm) and no greater than approximately 25 ppm of ozone (O_3).

[c3] The method of claim 2, wherein the ozonated water bath includes approximately 5 ppm of ozone (O_3).

[c4] The method of claim 1, wherein the exposing step includes exposing to ozonated water bath at a rate of approximately 30 standard liters per minute (slpm) of water (H_2O).

[c5] The method of claim 1, wherein the exposing step is conducted for no less than approximately 0.1 minutes and no greater than 10 minutes.

[c6] The method of claim 1, wherein the n-type dopant includes at least one of phosphorous and arsenic, and the p-type dopant includes at least one of boron and boron di-flouride.

[c7] The method of claim 1, wherein the exposing step generates an interfacial layer.

[c8] The method of claim 1, wherein the saliciding step includes:
depositing a metal layer;
depositing a cap layer on the metal layer;
annealing to form a silicide; and
removing the cap layer and excess metal layer.

[c9] A method for selectively forming silicide on a semiconductor device, the method comprising the steps of:
providing a PFET and an NFET; and
chemically pretreating at least the NFET to prevent silicide formation on the NFET.

[c10] The method of claim 9, wherein the pretreating step includes exposing at least the NFET to an ozonated water bath including no less than approximately 1 parts per

million (ppm) and no greater than approximately 25 ppm of ozone (O_3).

[c11] The method of claim 10, wherein the exposing step generates an interfacial layer.

[c12] The method of claim 10, wherein the exposing step includes exposing to the ozonated water bath at a rate of approximately 30 standard liters per minute (slpm) of water (H_2O) for approximately 5 minutes.

[c13] A method of forming a silicide portion of a semiconductor, the method comprising the steps of:
providing a first structure having an n-type dopant therein and a second structure having a p-type dopant therein;
chemically pretreating at least the NFET to prevent silicide formation on the NFET; and
salicidizing the first and second structure whereby silicide is formed only over the second structure.

[c14] The method of claim 13, wherein the pretreating step includes exposing at least the first structure to an ozonated water bath.

[c15] The method of claim 14, wherein the ozonated water bath includes no less than approximately 1 parts per million (ppm) and no greater than approximately 25 ppm

of ozone (O_3).

[c16] The method of claim 15, wherein the ozonated water bath includes approximately 5 ppm of ozone (O_3).

[c17] The method of claim 14, wherein the exposing step generates an interfacial layer.

[c18] The method of claim 14, wherein the exposing step includes exposing to the ozonated water bath at a rate of approximately 30 standard liters per minute (slpm) of water (H_2O) for no less than approximately 0.1 minutes and no greater than 10 minutes.

[c19] The method of claim 13, wherein the n-type dopant includes at least one of phosphorous and arsenic, and the p-type dopant includes at least one of boron and boron di-flouride.

[c20] The method of claim 13, wherein the salicidizing step includes:
depositing a metal layer;
depositing a cap layer on the metal layer;
annealing to form a silicide; and
removing the cap layer and excess metal layer.